

WHAT IS CLAIMED IS:

1. A method for forming a recognition mark on a substrate for KGD, wherein wiring patterns are formed on a surface of one side of an insulating substrate, comprising the steps of:

forming a conductive pattern as a recognition mark on one surface where said wiring patterns are formed; and

forming a through hole from a surface where said wiring pattern is not formed toward said conductive pattern.

2. A method for forming a recognition mark on a substrate for KGD as claimed in claim 1, wherein said substrate is formed with a bump to be connected to said KGD on the surface where said wiring pattern is not formed.

3. A method for forming a recognition mark on a substrate for KGD as claimed in claim 1, wherein said conductive pattern has a particular shape as said recognition mark.

4. A method for forming a recognition mark on a substrate for KGD as claimed in claim 1, wherein a shape of said through hole defines said recognition mark.

5. A method for forming a recognition mark on a substrate for KGD as claimed in claim 4, wherein said through hole

is filled with a plating material until the end of said plating lies in flush with said surface where said wiring pattern is not formed.

- 5 6. A method for forming a recognition mark on a substrate for KGD, wherein wiring patterns are formed on both surfaces of an insulating substrate, comprising the steps of:

forming a conductive pattern as a recognition mark
10 on one surface where said wiring patterns are formed; and

forming a through hole from a surface, where said KGD is not mounted and said wiring pattern is formed, toward said conductive pattern.

- 15 7. A method for forming a recognition mark on a substrate for KGD, wherein wiring patterns are formed on a plurality of layers of an insulating substrate, comprising the steps of:

forming a conductive pattern as a recognition mark
20 on any layer where said wiring patterns are formed; and

forming a through hole from a surface of the substrate where said KGD is to be mounted toward said conductive pattern.